Application No.: 09/540,828

REMARKS/ARGUMENTS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

It is noted that the Examiner did not consider an Information Disclosure Statement filed electronically on December 16, 2004. A copy is enclosed.

It is also note that the IDS faxed to the PTO was not considered by the Examiner. Apparently the form PTO/SB/08A did not scan correctly ***although the reference was placed in the electronic file***. A copy of the ***form*** is being sent again.

With regard to the provisional double patenting rejection, this issued will be addressed when allowable subject matter is found.

In reviewing the claims, it was noted that the term "messag*ing* network" and "message network" have been used interchangeably. In order for there to be consistency, the term "message network" was selected and therefore the term "messaging network" has been changed to "message network" throughout the claims.

The claims stand rejected under 35 USC 103(a) as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

It is Applicant's position, for reasons set forth in detail below that: (1) adding a global memory to Martin et al. would, contrary to the Examiner's assertion, reduce system bandwidth because such global memory is accessible by all directors and therefore would, with the Examiner's suggested arrangement, require arbitration among the directors for access to the shared, i.e., global memory; (2) the memory controller 208 of Gaskins is clearly a ***controller*** as shown in FIG. 3 of Gaskins and ***not a network***; (3) the controller 208 of Gaskins does not operate independently of the memory (after all it is the controller for the memory); and, (4) there is nothing in either Martin et al or Gaskins to suggest ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors such separation thereby removing the very arbitration requirement which would result from the Examiner's susgested arrangmrent***.

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More particularly, Applicant wished to make the following points:

1. Applicant has a global memory for storing user data. The global memory is accessible by all directors. Because all directors have access to the global memory for user data there is a requirement for arbitration to decide which one of multiple requesting directors has access to the memory. This arbitration for the memory by the plurality of directors ***reduces system bandwidth. Therefore, the Examiner's position that the use of a memory accessible by a plurality of directors increases bandwidth is not understood.***

2. With applicant's system of FIG. 2 and the prior system in FIG. 1, the control of the data between the host computer and disk drives is by processors in the directors. Thus, it is the plurality of directors that control the flow of data between the host computer and disk drives. The control in the applicant's system of FIG. 2 and the prior system in FIG. 1 is by messages which pass between the directors. In the prior system described in connection with FIG. 1 both the messages and user data went to the global memory. The Applicants recognized that the **bandwidth of the system of FIG. 1 could be increased** by having the message ***BY-PASS*** the global memory as described in FIG. 2. That is, the bandwidth of the system of FIG. 1 was increased because the messaging did not require the arbitration for access to the global memory as the data did for access to such memory. Thus, while the user data continued to pass to the global memory, ***the bandwidth was increased by having the messages BY-PASS the global memory.***

3. Reference is made to the first two paragraphs of the Summary section of the patent applications:

> In accordance with the present invention, a system interface is provided. Such interface includes a plurality of first directors, a plurality of second directors, a data transfer section and a message network. The data transfer section includes a cache memory. ***The cache memory is coupled to the plurality of first and second directors. The messaging network operates independently of the data transfer section and such network is coupled to the plurality of first directors and the plurality of second directors***. The first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network to facilitate data transfer between first directors and the second directors. The data passes through the

> cache memory in the data transfer section.
>
> With such an arrangement, ***the cache memory*** in the data transfer section ***is not burdened with the task of transferring the director messaging*** but ***rather*** a messaging ***network*** is provided, ***operative independent of the data transfer section,*** for such messaging *thereby* ***increasing the operating bandwidth*** *of the system interface.* (emphasis added)

4. Referring to Martin et al., there is no suggestion of ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors***. Examiner suggests adding the teaching of Gaskins to Martin et al., and refers to cache controller 208 of Gaskins as a message network. Cache controller 208 is just what it says, it ***is a controller***. ***The cache controller 208 does not pass messages through it between a plurality of directors. Further, the cache memory controller 28 is not operative independently of the data transfer section.***

With regard to Gaskins, reference is made to column 7, lines 29-38:

> Cache controller 208 ***orchestrates*** the transfer of control signals between CPU 202 and bus interface unit 210, and further manages the transfer of data between CPU 202, cache memory 206 and bus interface unit 210. Cache controller 208 partially consists of conventional logic circuitry that allows the cache memory 206 to be read, written, updated, invalidated and flushed. It should be noted that in the preferred form, CPU 202, cache memory 206 and cache controller 208 ***operate concurrently*** to provide maximum sustained performance in the computer system. (emphasis added)

It is first noted that cache controller 208 is clearly a ***controller*** which "***orchestrates*** the transfer " as distinguishes from a network which ***passes messages***; and is it next noted that cache controller 208 partially consists of conventional logic circuitry that allows the cache memory 206 to be read, written, updated, invalidated and flushed. It should be noted that in the preferred form, CPU 202, cache memory 206 and cache controller 208 ***operate concurrently*** and hence the cache controller 208 does not operate independently of the cache memory.

Thus, it is clear that: (1) the memory controller 208 a ***controller*** and ***not a network***;

(2) it does not operate independently of the memory (after all it is the controller for the memory); and, (3) there is nothing in either Martin et al or Gaskins to suggest ***separating*** user data from messages such that the messages used to control the flow of user data pass between one another through a message network so that the passing messages by-pass a global memory, ***such global memory being accessible for data by a plurality of directors***.

5. Neither the advantage nor the suggest to ***separate the control messages from the user data*** such that the ***user data goes through the global memory*** while the ***control messages pass between the directors through a message network and BY-PASS the global memory*** is not described or recognized in Martin et al. or Gaskins (U. S. Patent No. 5,903,911) taken either singly or in combination.

6. Neither the advantage nor the suggest to ***operate the message network independently of the data transfer section or global memory are*** described or recognized in Martin et al. or Gaskins (U. S. Patent No. 5,903,911) taken either singly or in combination.

Referring now to the claims, claim 1 points out that:

(1) such cache memory being ***coupled to the plurality of first and second directors***; and

(2) a message network, ***operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors;***

As noted above, the Examiner's position that the use of a memory accessible by a plurality of directors increases bandwidth is not understood because adding such a memory would require arbitartion for the memory by the directors thereby reducing bandwidth.

Thus, Applicant respectfully disagrees with the rejection of the claim 1-75 under 35 USC 103(a) as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

Claim 8 points out that:

(1) such ***cache memory*** being coupled to the plurality of first and second

directors;

(2) a message ***network***, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors;

Claim 15 points out that the method includes:

transferring messages through a message ***network*** with the data being transferred between the host computer/server and the bank of disk drives through ***a cache memory***, such ***message network being independent of the cache memory***.

Claim 16 points out that the method includes:

transferring the data between the host computer/server and the bank of disk drives under control of the first and second directors in response to ***messages passing between the first directors and the second directors through a message network*** to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the ***cache memory*** in the data transfer section, ***such message network being independent of the cache memory***.

Claim 17 points out that the method includes:

providing a message network, ***operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors*** to control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through ***the cache memory*** in the data transfer section.

Claim 25 points out that the system includes:

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(1) such cache memory ***being coupled to the plurality of first and second directors***;

(2) a message network comprising ***a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of first directors and second directors***, such message network ***being operative independently of the data transfer section***; and

(3) wherein the first and second directors control data transfer between the first directors and the second directors in response to ***messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors*** with such data passing through the cache memory in the data transfer section.

Claim 16 points out that the interface includes:

(1) such ***cache memory being coupled to the plurality of first and second directors***;

(2) ***a message network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors***;

Claim 28 points out that the interface includes:

(***1) such cache memory being coupled to the plurality of first and second directors;***

(***2) a message network coupled to the plurality of first directors and the plurality of second directors;*** and

(3) such messages ***by-passing*** the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

Claim 30 points out that the intercae includes:

(1) ***such cache memory being coupled to the plurality of first and second***

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directors;

(2) a message ***network*** comprising a switch network having a plurality of ports, each one of the ports being ***coupled to a corresponding one of the plurality of first and second directors***; and

(3) with such messages ***by-passing*** the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

Claim 31 points out:

(1) ***such cache memory being coupled to the plurality of directors***;

(2) a message ***network, operative independently of the data transfer section***, coupled to the plurality of directors

Claim 35 points out:

(1) such cache memory ***being coupled to the plurality of first and second directors***;

(2) a message network, ***operative independently of the data transfer section***, coupled to the plurality of first directors and the plurality of second directors; and

Claim 39 points out:

such cache memory ***being coupled to the plurality of directors***;

a message ***network***, ***operative independently of the data transfer section***, coupled to the plurality of directors

Claim 43 points out:

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(1) ***such cache memory being coupled to the plurality of directors***;

(2) a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors, such message network being ***operative independently of the data transfer section***;

Claim 43 points out:

such cache memory being coupled to the plurality of directors;

a message network, ***operative independently of the data transfer section***, coupled to the plurality of directors

Claim 46 points out:

such cache memory being coupled to the plurality of directors;

a message network coupled to the plurality of directors; and

wherein the first and second directors control data transfer in response to messages passing between the directors through the message network with such messages ***by-passing the data transfer section*** and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

Claim 48 points out:

such cache memory ***being coupled to the plurality of directors***;

a message network comprising a switch network having a plurality of ports, each one of the ports being coupled to a corresponding one of the plurality of directors; and

wherein the directors control data transfer in response to messages passing between the directors through the message network with such messages ***by-passing*** the

data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section.

Claim 49 points out:

such cache memory being ***coupled to the plurality of directors;***

a message network, ***operative independently of the data transfer section,*** coupled to the plurality of directors

Claim 53 points out:

such cache memory being coupled to the plurality of first and second directors;

a message ***network, operative independently of the data transfer section,*** coupled to the plurality of first directors and the plurality of second directors; and

Claim 57 points out:

a cache memory ***coupled to the first director and the second director;***

a message ***network*** coupled to the first director and the second director;

wherein the first and second directors control data transfer between first director and the second director with the data in the data transfer passing through the cache memory in response to messages passing between the first director and the second director ***through the message network;*** and

wherein the messages passing through the message network ***by-pass*** the cache memory..

Claim 58 points out:

a message ***network*** coupled to the first director and the second director;

wherein the first and second directors control data transfer between first director and the second director with data in ***such data transfer passing through the cache memory*** in response to messages passing between the first director and the second director through the message network; and

wherein each one of the messages includes a destination field.

Claim 59 points out:

such cache memory being ***coupled to the plurality of first and second directors***;

a message ***network*** coupled to the plurality of first directors and the plurality of second directors;

wherein the messages passing through the message network ***by-pass*** the cache memory.

Claim 60 point out:

a message network coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the host computer and the bank of disk drives with data in such **data transfer passing through the cache memory in response to messages passing between the first director and the second director through the message network**; and

wherein each one of the messages includes a destination field.

Claim 61 points out:

the cache memory is ***coupled the plurality of first directors and to the plurality of second directors***;

wherein data is transferred between first directors and the second directors through the cache memory in response to messages passing between the first directors and the second directors through the message ***network***; and

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wherein the messages passing through the message network ***by-pass*** the cache memory.

Claim 63 points out:

wherein data is transferred between the first directors and the second directors ***through the cache memory*** in response to ***messages passing*** between the first directors and the second directors ***through*** the message ***network***

Claim 64 points out:

a message ***network***, coupled to the first director and the second director;

wherein where the cache memory ***is coupled the first director and to the second director***;

wherein data is transferred between the first director and the second director through the cache memory in response to ***messages passing between the first director and the second director through*** the message ***network***; and

wherein the messages passing through the message network ***by-pass*** the cache memory.

Claim 66 points out:

wherein data is transferred between the first director and the second director through ***the cache memory*** in response to ***messages*** passing between the first director and the second director ***through the message network***; and

wherein each one of the messages comprises a packet, such packet having a destination field.

Claim 67 points out:

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a cache memory coupled to the data ports of the plurality of directors;

a message network coupled to the message ports of the plurality of directors;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors ***through*** the message ***network***; and

wherein the messages passing through the message network ***by-pass*** the cache memory.

Claim 69 points out:

a cache memory ***coupled to the plurality of directors***;

a message ***network*** coupled to the message ports ***of the plurality of directors***;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors ***through*** the message ***network***; and

wherein with messages passing through the message network ***by-pass*** the cache memory.

Claim 72 point out:

a cache memory ***coupled to the plurality of directors***;

a message ***network*** coupled to the ***message ports*** of the plurality of directors;

wherein the plurality of directors control data transfer in response to said messages passing between the directors, each one of said messages including a destination field.

Claim 73 point out:

a cache memory ***in communication with the plurality of directors;***

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a message ***network*** coupled to the message ports of the plurality of directors;

wherein the plurality of directors control data transfer between the directors with said data in such data transfer passing through the cache memory in response to said messages passing between the directors through the message network; and

wherein the messages passing through the message network ***by-pass*** the cache memory.

Claim 75 points out:

a cache memory ***in communication the plurality of directors***;

a message network ***coupled to the message ports of the plurality of directors***;

wherein the plurality of directors control data transfer in response to said messages passing between the directors, each one of said messages includes a destination field.

As noted above, the Examiner's position that the use of a memory accessible by a plurality of directors increases bandwidth is not understood because adding such a memory would require arbitartion for the memory by the directors thereby reducing bandwidth.

Thus, Applicant respectfully disagrees with the rejection of the claim 1-75 under 35 USC 103(a) as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 05-0889.

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